REMARKS

The present application was filed on October 20, 2003, with claims 1-20. Claims 1-20 remain pending. Claims 1 and 18-20 are the independent claims.

Claims 1-8, 11 and 14-20 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2002/0176357 (hereinafter "Lay").

Claims 9 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lay in view of U.S. Patent Publication No. 2005/0278503 (hereinafter "McDonnell").

Claims 12 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lay in view of U.S. Patent Publication No. 2002/0075540 (hereinafter "Munter").

With regard to the §102(e) rejection, Applicants respectfully note that MPEP §2131 specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In formulating the present rejection, the Examiner further argues that Lay discloses the limitations of claim 1 wherein a flow control message is generated in the physical layer device and transmitted from the physical layer device to the link layer device. Specifically, the Examiner contends that gigabit interface 104 in FIG. 1 is a physical layer device which generates a flow control message, which is then transmitted to a flow control manager 116 allegedly located in the MAC of ports 102(1)-102(12).

In arguing that gigabit interface 104 is a physical layer device which generates a flow control message, the Examiner relies primarily on paragraph [0031] of Lay:

> Gigabit interface 104, like ports 102(1)-102(12), has a PHY, a Gigabit Media Access Controller (GMAC) and a latency block. The GMAC can be a fully compliant IEEE 802.3z MAC operating at 1 Gbps full-duplex only and can connect to a fully compliant GMII or TBI interface through the PHY. In this example, GMAC 108 provides full-duplex flow control mechanisms and a low cost stacking solution for either twisted pair or TBI mode using in-band signaling for management.

Applicants respectfully submits that the relied-upon portion of Lay in fact discloses that gigabit interface 104, like ports 102(1)-102(12), comprises a physical layer device (PHY) and a link layer device (GMAC). It should be noted that, in the previous Office Action, the Examiner correctly indicates FIG. 1A of Lay shows a plurality of ports 102(1)-102(12), each of which comprises a physical layer device (physical element PHY) and a link layer device (Media Access Controller MAC). See also Lay at [0026] and [0027].

Moreover, because the GMAC can only connect to a fully compliant GMII or TBI interface through the PHY, the GMAC is not "a device which provides an interface between a link layer device and a physical transmission medium of a network-based system" and hence not a physical layer device. Thus, even if the disclosure of Lay at [0031] of a GMAC which provides full-duplex flow control mechanisms could be construed as teaching that a GMAC within gigabit interface 104 generates a flow control message, this would nonetheless fail to teach or even suggest the limitation wherein a flow control message is generated in the physical layer device.

Applicants respectfully submit that the new embodiment of Lay relied upon in the present rejection fails to disclose the aforementioned limitations of claim 1 for reasons similar to those presented in Applicants' response filed January 9, 2008, which the Examiner deemed persuasive.

The Examiner further contends that a comparison of paragraph [0028], lines 1-4 ("Flow control is provided by each of the MACs" located in the ports), and paragraph [0039], lines 1-2 ("Switch 100, in one example of the invention, has a Flow Control Manager 116 that manages the flow of packet data") indicates that Flow Control Manager 116 is located in the MAC of a port. Applicants respectfully disagree and instead submit that the MACs within port 102(1)-102(12) and the Flow Control Manager 116 are instead distinct components of switch 100 which are involved in flow control.

Additional evidence may be found in FIG. 1A of Lay, which clearly shows Flow Control Manager 116 as being a distinct component rather than located within the MAC of ports 102(1)-102(12). See also Lay at [0051]-[0052] ("Each of the transmit (TX) and receive (RX) portions of ports 102(1)-102(12) are connected to the PBM Bus, ATM Bus, and TXM Bus for communications with other components of the switch. . . . [The Flow Control Manager 116 is] also connected to the ATM Bus for communications with other portions of the switch.")

Notwithstanding the above traversal, Applicants have amended independent claims 1 and 18-20 without prejudice to include limitations wherein the flow control message is responsive to a detected condition relating to at least a given one of a plurality of egress queues of the physical layer device and wherein the link layer device is operative to alter a characteristic of a flow of data from the link layer device to the physical layer device responsive to backpressure information in the flow control message. Support for the present amendments may be found in the specification at, for example, page 2, line 22, to page 3, line 13; page 10, line 12, to page 11, line 19; and page 19, lines 13-15.

Rather than teaching the claimed techniques wherein a flow control message is responsive to a detected condition relating to an egress queue of a physical layer device and wherein the link layer device is operative to alter a characteristic of a flow of data from the link layer device to the physical layer device responsive to backpressure information in the flow control message, the flow control described by Lay is directed to managing the flow of incoming data packets from a port to a switch. See, for example, Lay at [0028] ("Flow control is provided by each of the MACs. When flow control is implemented, the flow of incoming data packets is managed or controlled to reduce the chances of system resources being exhausted.")

See also Lay at [0039] ("Switch 100 . . . has a Flow Control Manager 116 that manages the flow of packet data. As each port sends more and more data to the switch, Flow Control Manager 116 can monitor the amount of memory being used by each port 102(1)-102(12) of switch 100 and the switch as a whole.") and Lay at [0074] (Flow Control Manager (FCM) 116 "monitors the ATM Bus to determine how much memory is being used to store data and how much memory is free for storing data. Based on this information, FCM 116 can send commands to each port . . . . requesting that the port slow down the sending of packet data to memory.")

Accordingly, Lay fails to teach, or even suggest, the limitations of amended claim 1. Independent claims 18-20 have been amended in similar fashion to independent claim 1 and thus believed to be patentable for at least the reasons identified above in reference to claim 1.

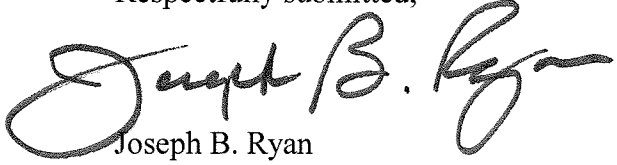
Dependent claims 2-17 are believed allowable for at least the reasons identified above with regard to independent claim 1, from which they depend. Moreover, one or more of these claims are believed to define separately patentable subject matter.

For example, dependent claim 6 includes a limitation wherein the flow control message comprises a logical MPHY value corresponding to the given queue. As described in the specification at, for example, page 1, lines 24-26, an MPHY is one of the multiple channels over which a multiple-port physical layer device may communicate with a link layer device. See also page 11, lines 8-10. As described in the present specification at, for example, page 5, line 22, to page 6, line 5, the inclusion of the logical MPHY value in the flow control message provides a number of advantages.

The Examiner contends that this limitation is met by Lay at [0070], lines 4-7. See the present Office Action at page 4, first paragraph. Applicants note that the relied-upon portion of Lay discloses that "TXM Memory is allocated on a per port basis so that if there are ten ports there are ten queues within the TXM Memory allocated to each port." Applicants respectfully submit that the relied-upon portion of Lay fails to teach, or even suggest, the limitation of dependent claim 6 wherein the flow control message comprises a logical MPHY value corresponding to the given queue.

In view of the above, Applicants believe that claims 1-20 are in condition for allowance, and respectfully request the withdrawal of the §102(e) and §103(a) rejections.

Respectfully submitted,



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